



Fact Sheet: Design Forward

Objective

The objective of the Design Forward program is to initiate public-private partnerships with DOE Laboratories and vendors, funded jointly by the Department of Energy's Office of Science (SC) and the National Nuclear Security Administration (NNSA). The partnerships will accelerate the research and development of critical technologies needed for extreme-scale computing systems to meet the Department's mission needs.

Research Areas Supported

The principal research areas in Design Forward are system integration and interconnect technology.

- On April 9, 2015, DOE will announce \$10M in Design Forward Phase 2 awards to four vendors -- AMD, Cray, IBM and Intel Federal -- which will complement and build on the Design Forward phase 1 awards. The vendors will:
 - Develop and evaluate a proposed execution model, the crosscutting set of computational rules, and relations that guide co-design of the computer system component layers and govern their interoperability;
 - Develop conceptual system design(s), including hardware and software, targeted at Exascale systems to be delivered in the 2023 timeframe;
 - Conduct an alternatives analysis of expected component technology options and identify features that are needed from component developers for successful system integration;
 - Collaborate with DOE's Exascale Co-design Centers to determine how changes in system architectures will affect the scientific applications performed on the next generation of supercomputers.

- Previously, on November 15, 2013, the Department announced Design Forward Phase 1 awards totaling \$25.4M to five vendors to support the design and evaluation of interconnect architectures for future high performance computing (HPC) resources.
 - Interconnect and tie together hundreds of thousands of processors as building blocks of supercomputers. Design Forward's focus is on developing interconnects that are energy efficient, have high bandwidth, and minimize the time to move data among processors.
 - Vendors and the areas supported include:
 - Intel: Interconnect architectures and implementation approaches
 - Cray: Open Network protocol standards
 - AMD: Interconnect Architectures
 - IBM: Energy-efficient interconnect architectures
 - NVIDIA: Interconnect architectures for massively threaded processors